



Aviation Safety Program

Integrated Vehicle Health Management Technical Accomplishments

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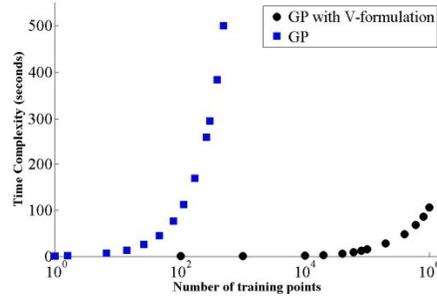
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ARMD Review
NASA Headquarters
November 5, 2007



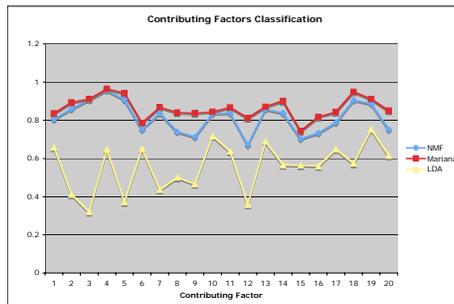
Key Accomplishments



Highly Scalable Prognostics
*(Inverting Matrices with 10^{12} elements
 MS 1.8.5, 2.8.3)*

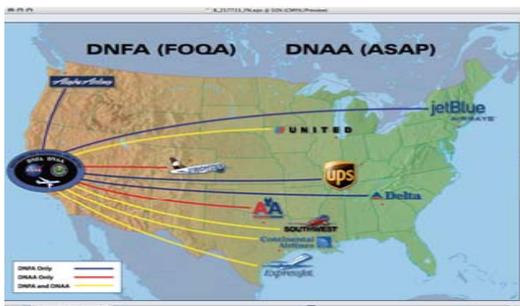
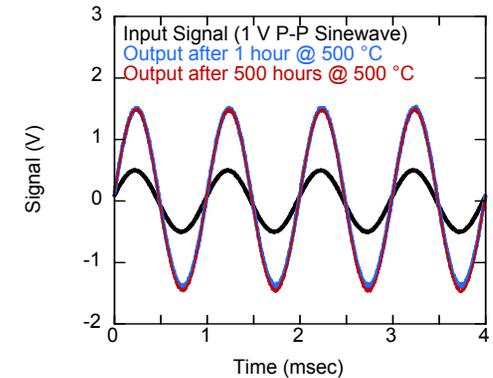


Bayesian Modeling for Diagnostics
*(Operating in a state space of size 2^{400} in
 millisecond time, MS 1.4.1, 1.4.5, 2.4.3, 3.4.2)*



Automatic Identification of Contributing Factors for Aviation Incidents
(No supervised training required, MS 3.82, 2.84, 1.8.5)

High Temperature Technologies
*(3000 Hours of World Record
 Performance, MS 1.3.5)*



Transfer of Distributed National FOQA and ASAP
 Archives to FAA
*(Enabling Fleetwide IVHM through Data Mining,
 PART Milestone FY07)*



Aviation Safety Program

Bayesian Methods for Diagnosis

Ole J. Mengshoel, Ph.D

NASA Ames team:

- Scott Poll
- Ann Patterson-Hine
- David Garcia
- David Hall
- Charles Lee
- Chris Neukom
- David Nishikawa
- John Ossenfort
- Adam Sweet
- Serge Yentus
- Serdar Uckun

UCLA team:

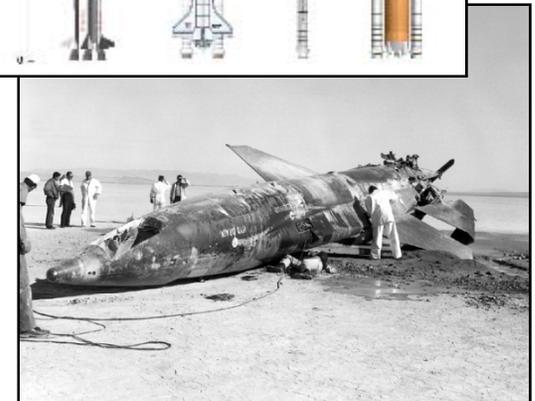
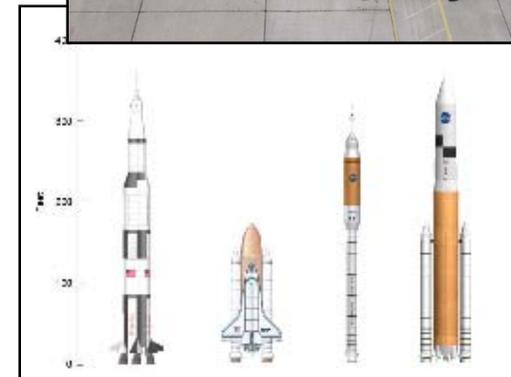
- Adnan Darwiche
- Keith Cascio
- Mark Chavira
- Yuliya Zabiyaka

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Integrated Vehicle Health Management

- Real-time operating system (RTOS) used in current avionics:
 - Task has: period, deadline, and worst-case execution time (WCET)
 - Priority-based preemptive scheduling
- The challenge of embedding AI into a hard real-time system:
 - Difficulty of the computational problems
 - High expectation and/or variance of a search algorithm's execution time
- Embedded IVHM processes for diagnosis, sensor validation, prognosis:
 - Should be designed within RTOS resource bounds – such as WCET
 - Involve uncertainties – probability of component and sensor failure



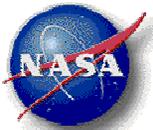


Uncertainty and Bayesian Reasoning

- Need to represent and reason with uncertain data in IVHM
- Uncertainty reasoning based on probability theory is well-established
- Earlier: Probability theory is elegant, *but has serious limitations*:
 - Requires too much information – joint distribution is exponentially large
 - Inefficient and unpredictable algorithms
 - Is unsuitable for embedded IVHM
- Recently: *Solutions* to above issues
 - Hardware speed
 - Bayesian networks (BNs) that decompose the joint distribution
 - Efficient algorithms: Compilation of BN to arithmetic circuit, where computation is fast and predictable

Bayesian Reasoning for Diagnostics: *Operates in a state space of size $> 2^{400}$ in time less than one millisecond.*

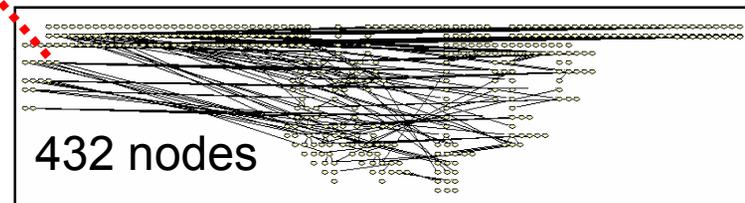




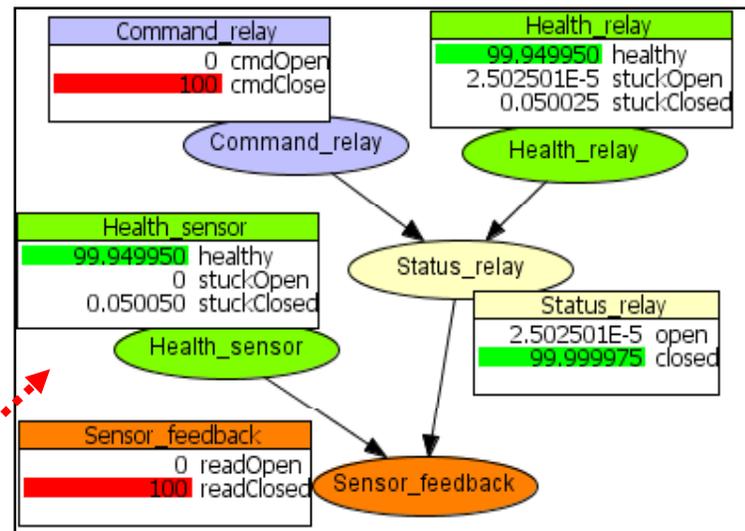
Our Bayesian Diagnosis Approach

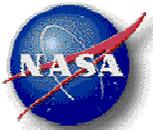


- Bayesian network model for a vehicle's subsystem(s):
 - It represents health of sensors and subsystem components explicitly
 - It contains random variables for other parts of the subsystem
- A Bayesian approach to:
 - *Diagnosis*: health status of system component nodes
 - *Sensor validation*: health status of sensor nodes

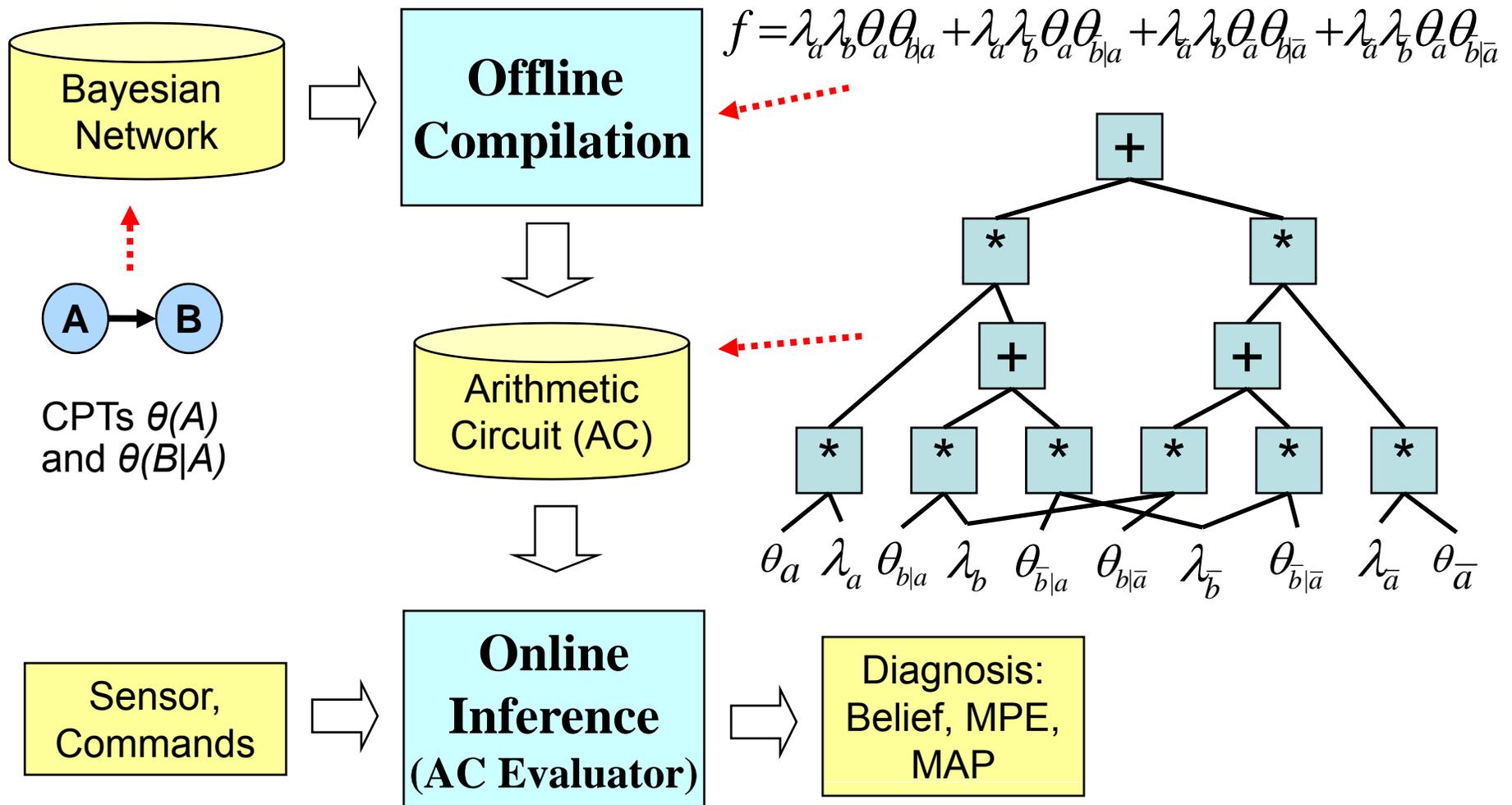


Much simplified but illustrative example





Compilation Approach to Diagnosis

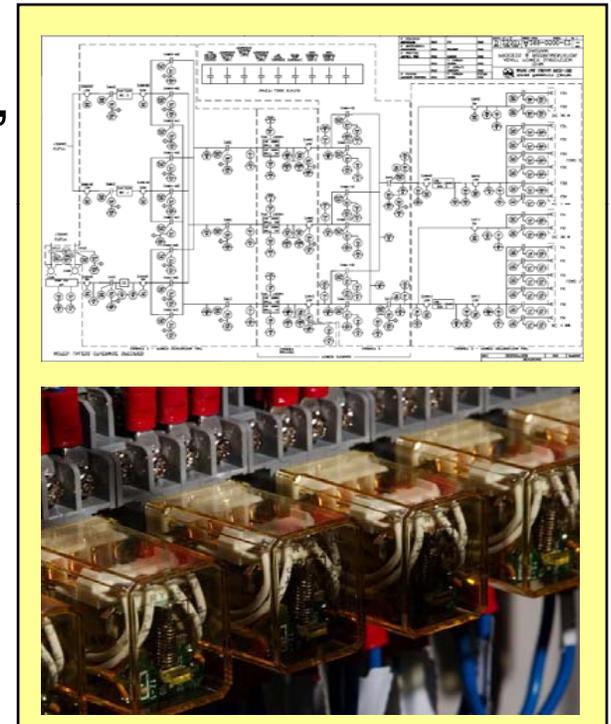


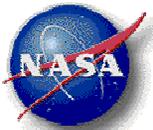
For details on Arithmetic circuits: [Darwiche, 03; Darwiche & Chavira, 07]



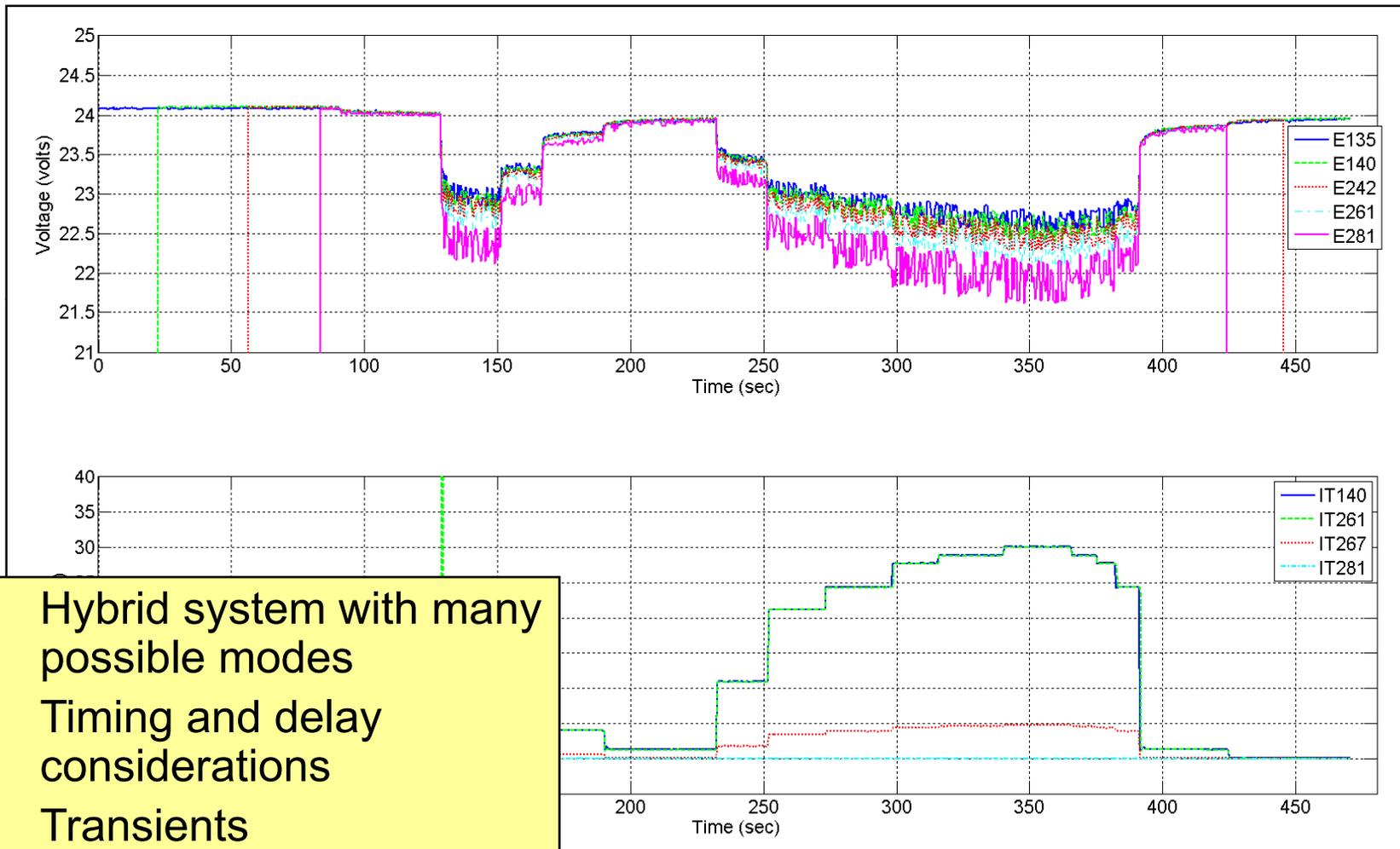
ADAPT Testbed

- ADAPT: Electrical power system (EPS) testbed developed at NASA Ames
- EPS loads include: avionics, propulsion, life support, and thermal management
 - Increased reliance on EPS in new air- and spacecraft
- ADAPT provides:
 - a *standard testbed* for evaluating diagnostic algorithms & software;
 - a capability for controlled insertion of faults, giving *repeatable failure scenarios*; and
 - a *stepping stone* for maturing diagnostic technologies.

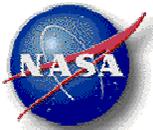




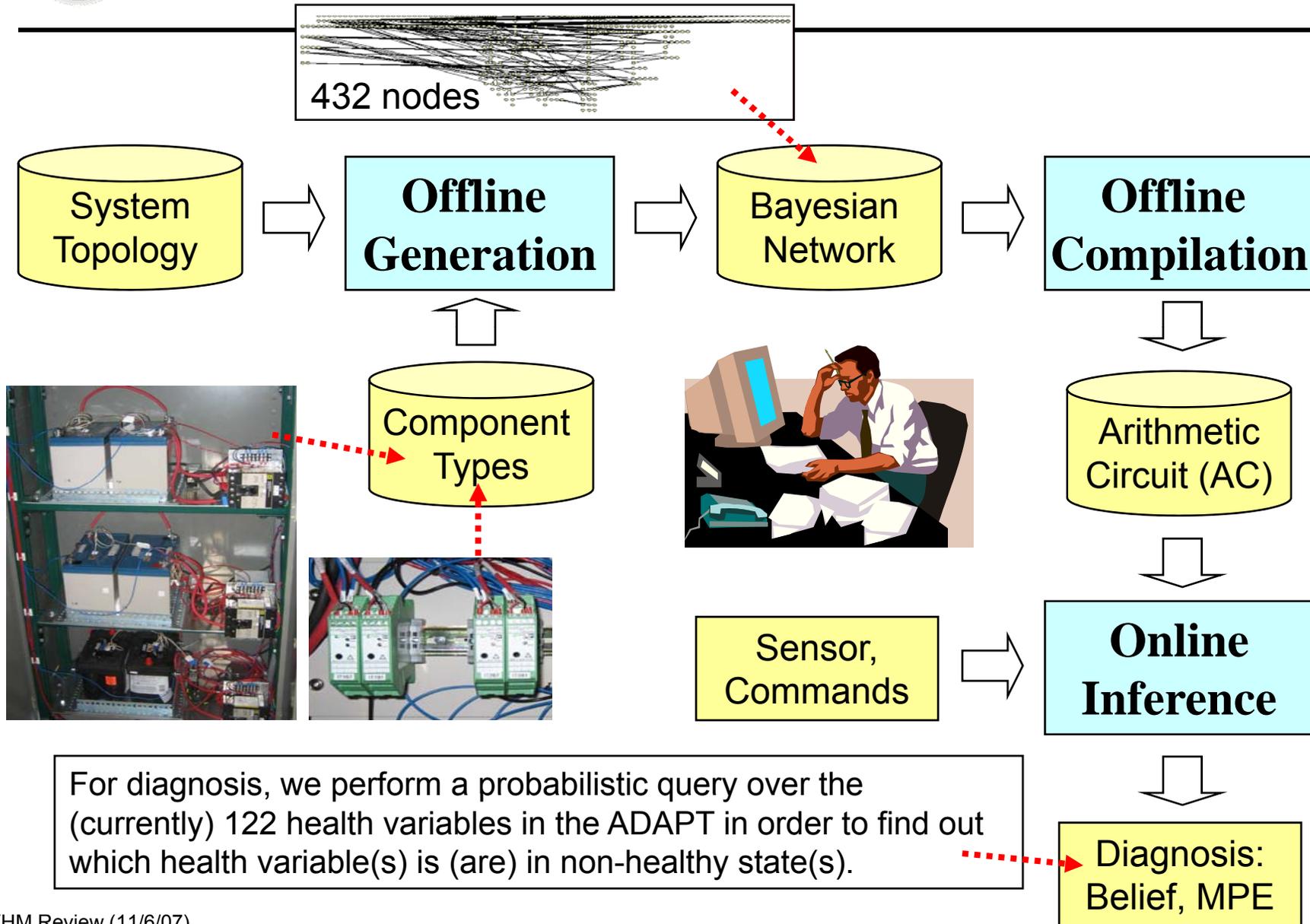
EPS: Diagnostic Challenges



- Hybrid system with many possible modes
- Timing and delay considerations
- Transients
- Load-dependent noise



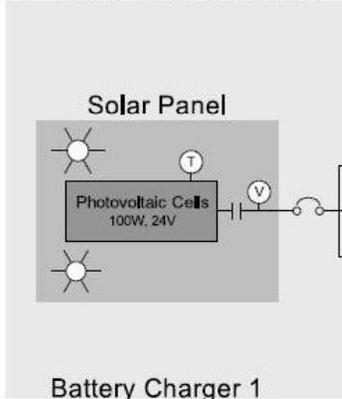
Compilation for Diagnosis in ADAPT



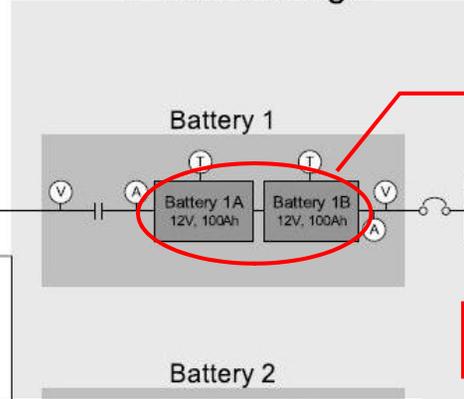


ADAPT Fault Injection Experiments

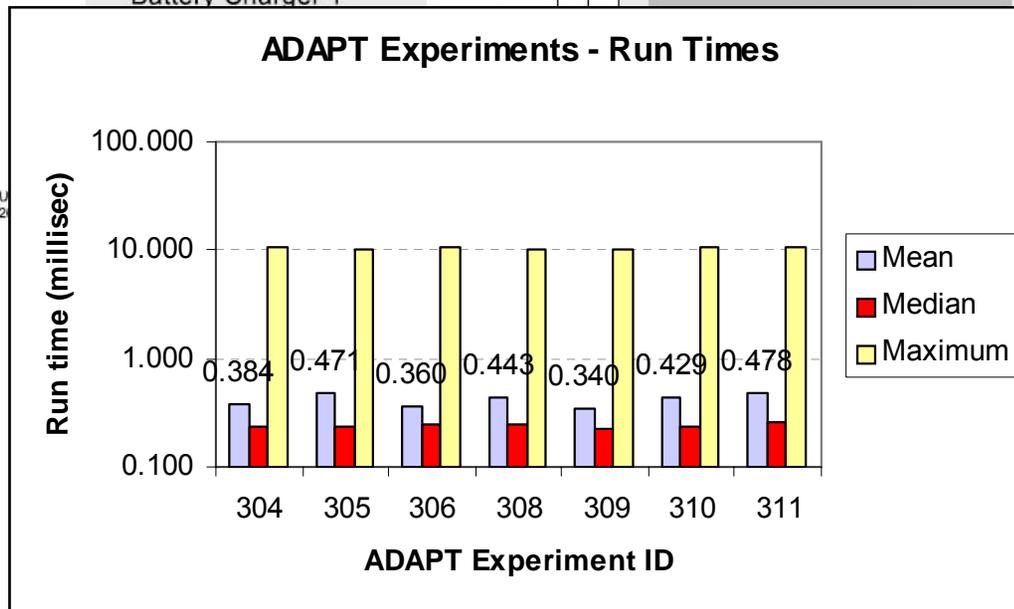
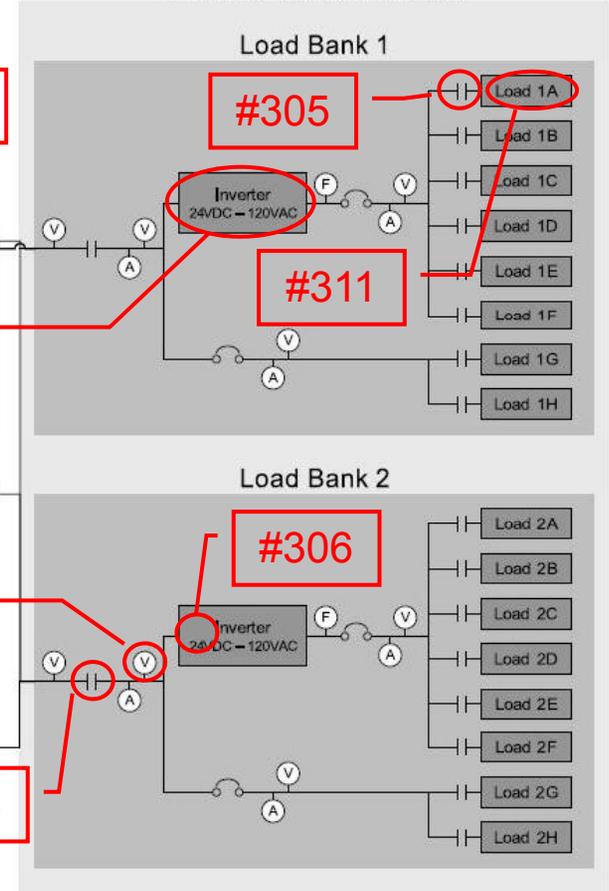
Power Generation



Power Storage



Power Distribution





Summary

- IVHM challenges:
 - Complex systems, large state spaces
 - Uncertainty - components and sensors may fail
 - Computationally hard problems
 - Resource-bounds – real time requirements
- Successful application of Bayesian networks in ADAPT:
 - Diagnosis and sensor validation under uncertainty
- Benefits of compilation to arithmetic circuit:
 - *Speed*: 300-400 microseconds (on average, in software) for ADAPT
 - *Predictability*: important for real-time IVHM applications

Bayesian Reasoning for Diagnostics: *Operates in a state space of size $> 2^{400}$ in time less than one millisecond.*





IVHM Technical Accomplishment

High Temperature SiC Transistor Integrated Circuits

Philip Neudeck, Gary Hunter, Robert Okojie, Glenn Beheim,
Roger Meredith, Terry Ferrier, Laura Evans, Michael Krasowski,
and Norman Prokop

NASA Glenn Research Center

<http://www.grc.nasa.gov/WWW/SiC/>

David Spry and Liang-Yu Chen

OAI

Dorothy Lukco and Carl Chang

ASRC

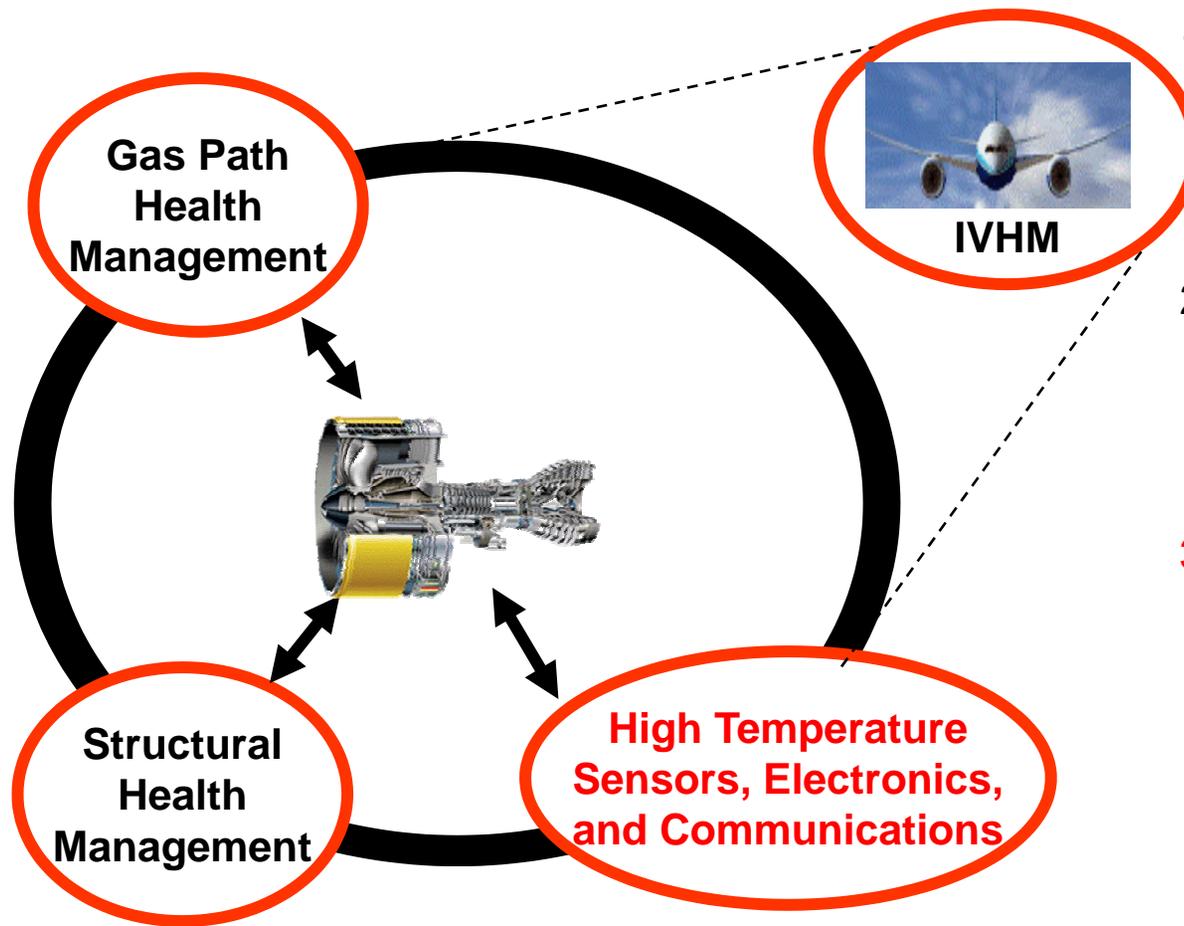
Aviation Safety Program Review

6 November 2007



IVHM - Propulsion Health Management

Task 3.3: High-Temperature Enabling Technologies



“Sensor development will be focused in three primary areas:

- 1) high-temperature pressure sensors for incorporation into gas-path trending and fault diagnostic models to infer turbine health,
- 2) structural health monitors including smart accelerometers, and optical strain and blade tip-timing sensors, and
- 3) **high-temperature wireless communications and energy harvesting technologies to enable the addition of these high-temperature sensors while minimizing wiring and power requirements on the engine.”**



Enabling Technology

High Temperature Integrated Circuitry

High temperature semiconductor integrated circuit (IC) chips are the key foundational technology for realizing health management technologies in harsh environments.

Once developed, high-temperature semiconductor IC chips could:

- be physically small and light (to put as many as you need, anywhere they are needed).
- be highly complex to perform “intelligent” circuit functions.
- operate with relatively low power consumption.
- operate in hot engine areas without active liquid coolant plumbing/lines.
- communicate data wirelessly (to FADEC, or other “distributed control” chips).

CRITICAL REQUIREMENT: High temperature electronic IC’s must operate DURABLY AND RELIABLY in order to be useful to most applications.

Temperatures exceed 300 °C in important areas of engines.

Peak compressor gas T near 500 °C, higher for combustor & exhaust.

Above 300 °C ambient, wide bandgap semiconductors (SiC) are needed.

- Beyond physical limits of silicon IC’s (including “high T” silicon chips).
 - Adverse silicon leakage currents - loss of “semiconductor” behavior.
 - Chemical diffusions and reactions (this is also a problem for GaN).
- Active (liquid) electronics cooling **negatively offsets** desired system benefits.



High Temperature Semiconductor Electronics

Of the examples of semiconductor transistor integrated circuit demonstrations in published literature, none prior to this work demonstrated stable electrical operation beyond a few hours at $T \geq 500\text{ }^{\circ}\text{C}$.

Initial Goal: Highly durable 500-600 $^{\circ}\text{C}$ integrated circuit technology foundation.

- Prolonged operation without cooling, physically small, up-scalable.
- Sensor signal conditioning and data transmission (wireless).

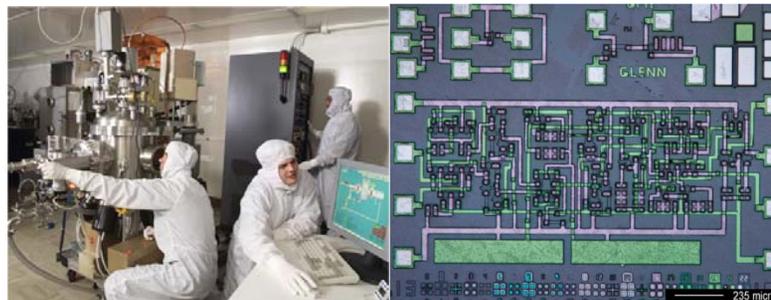
NASA's UNIQUE RANGE OF HARSH ENVIRONMENT TECHNOLOGY AND CAPABILITIES

Range of Physical and Chemical Sensors for Harsh Environments

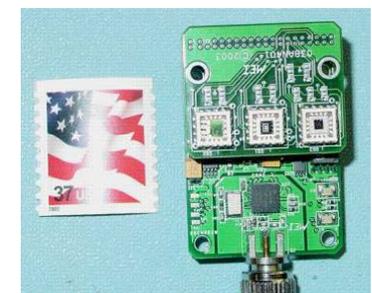


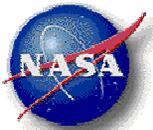
IVHM Review (11/6/07)

Microfabrication Laboratory SiC Clean Room Processing



Intelligent Sensor Mini-Systems

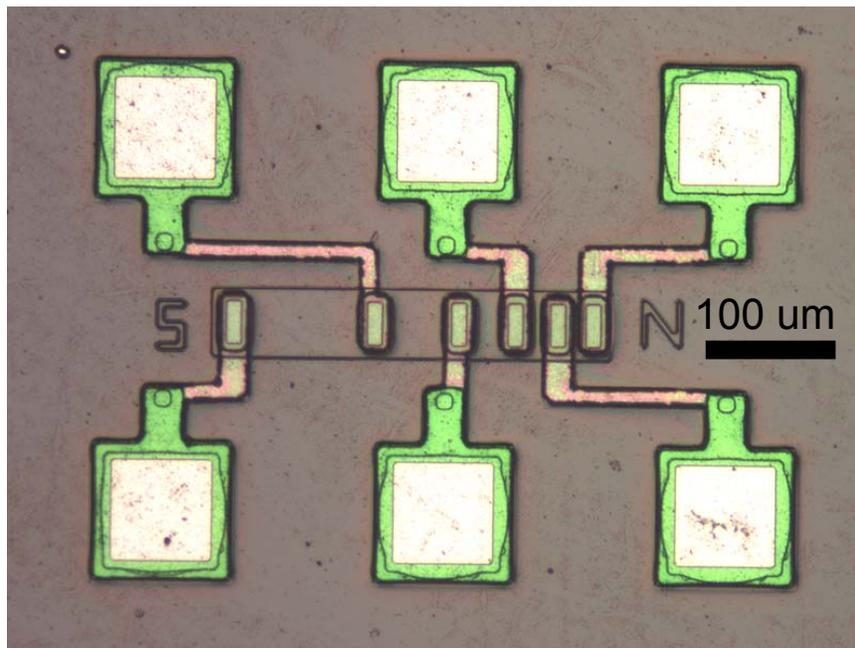




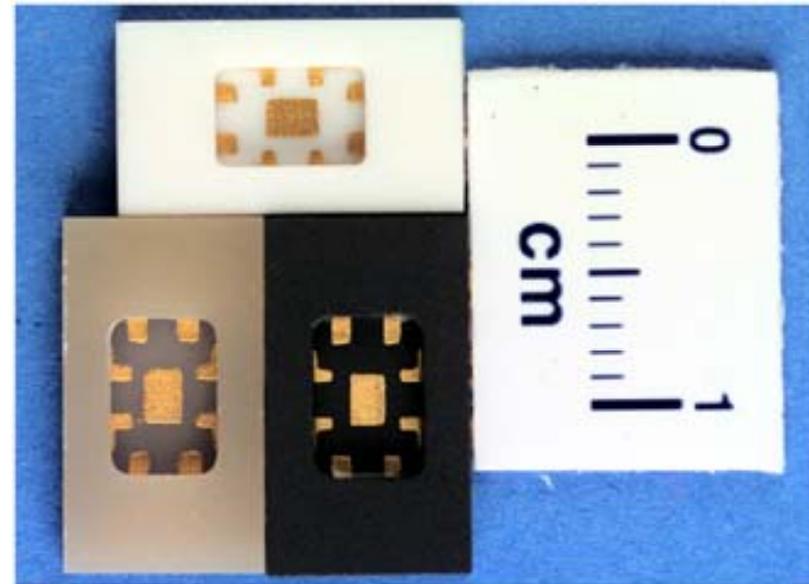
Previous (to IVHM) Key NASA Glenn Advancements

Key fundamental high temperature electronic materials and processing challenges have been faced and overcome by systematic basic materials processing research (fabrication and characterization).

500 ° C Durable Metal-SiC Contacts
(R. Okojie, 2000 GRC R&T Report)



500 ° C Durable Chip Packaging
And Circuit Boards
(L. Chen, 2002 GRC R&T Report)

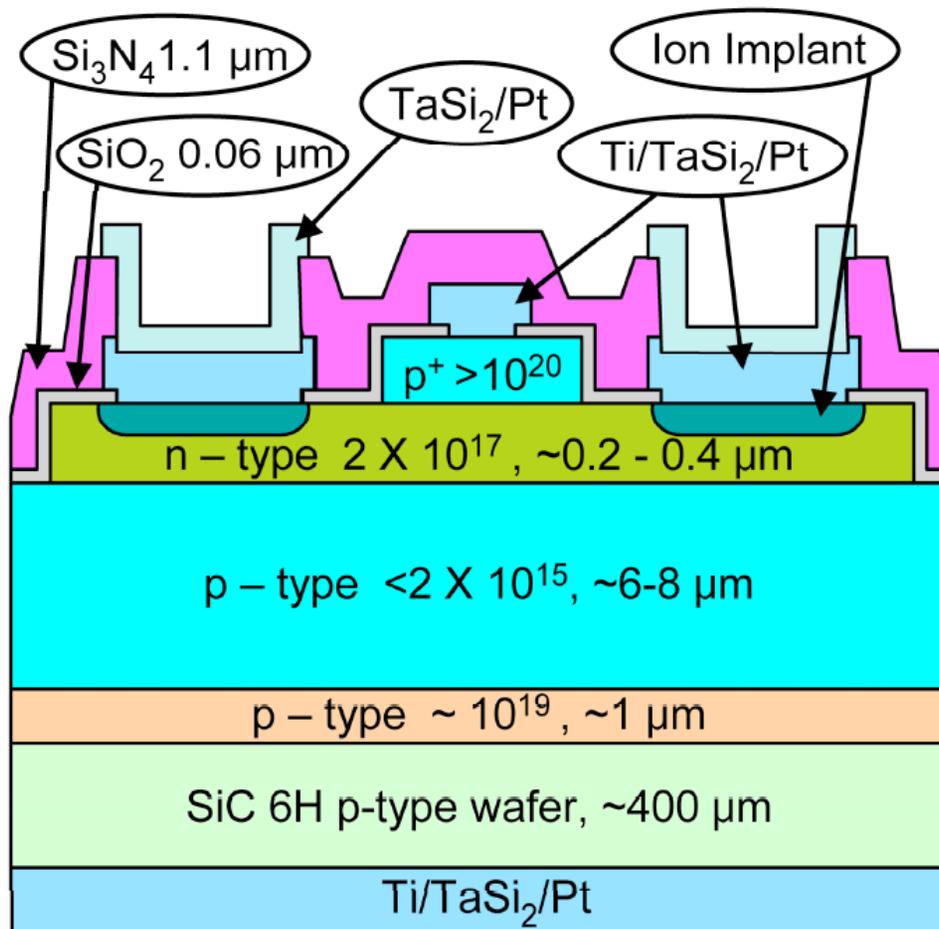


Additional advancements in device design, insulator processing, etc. also made.



SiC Transistor Structure

6H-SiC Junction Field Effect Transistor (JFET)



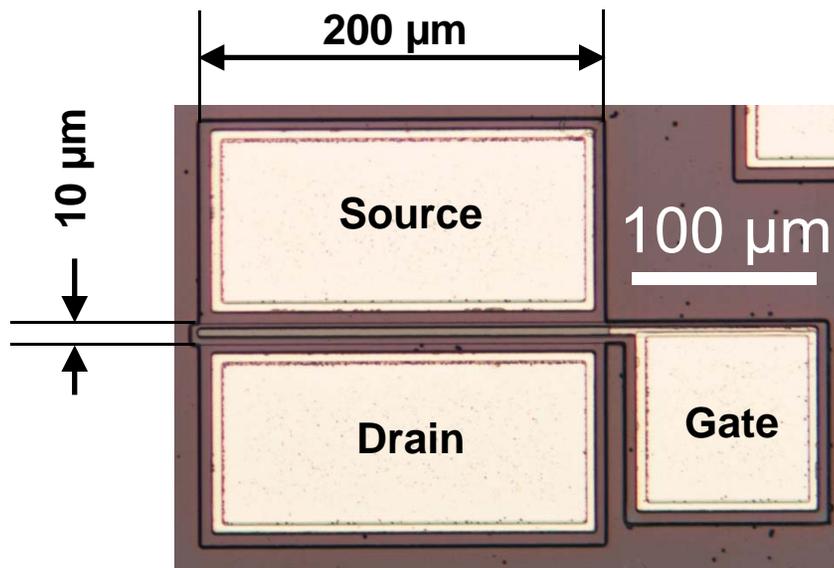
- 6H p-type SiC wafer with epilayers (purchased from Cree)
- Two p-type epilayers
 - ~ 10^{19} , ~ 1 μm (buffer layer)
 - ~ 10^{15} , ~ 6-8 μm
- n-type channel
 - 1-2 $\times 10^{17}$, ~0.2-0.4 μm
- p⁺ gate ~ 10^{20} , ~ 0.14 μm
- Ti/TaSi₂/Pt electric contact
- Oxide (wet rewet) and nitride passivation
- Triple-layer contact on the backside of wafer
- TaSi₂/Pt interconnect metal (single layer interconnect)
- Metal patterning was dry/wet no ion damage to dielectric

JFET chips enabled by development and integration of new SiC processes.



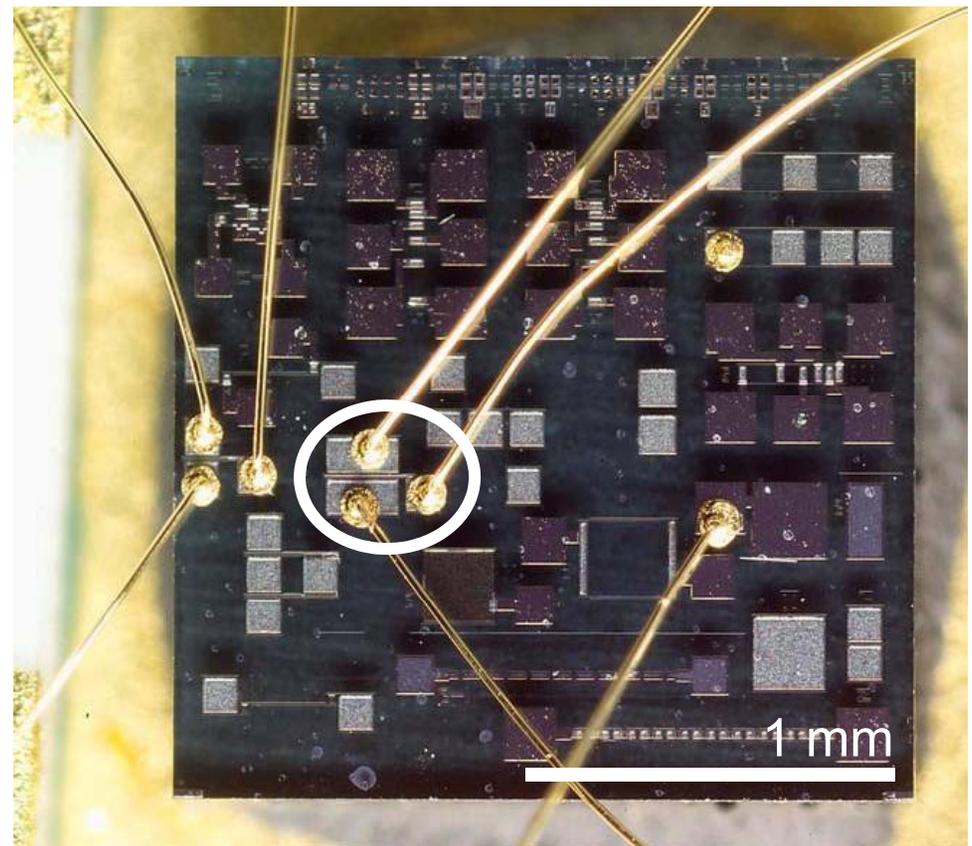
6H-SiC Junction Field Effect Transistor (JFET) Fabricated by NASA Glenn Research Center

200 μ m/10 μ m 6H-SiC JFET



Optical micrograph of device before packaging

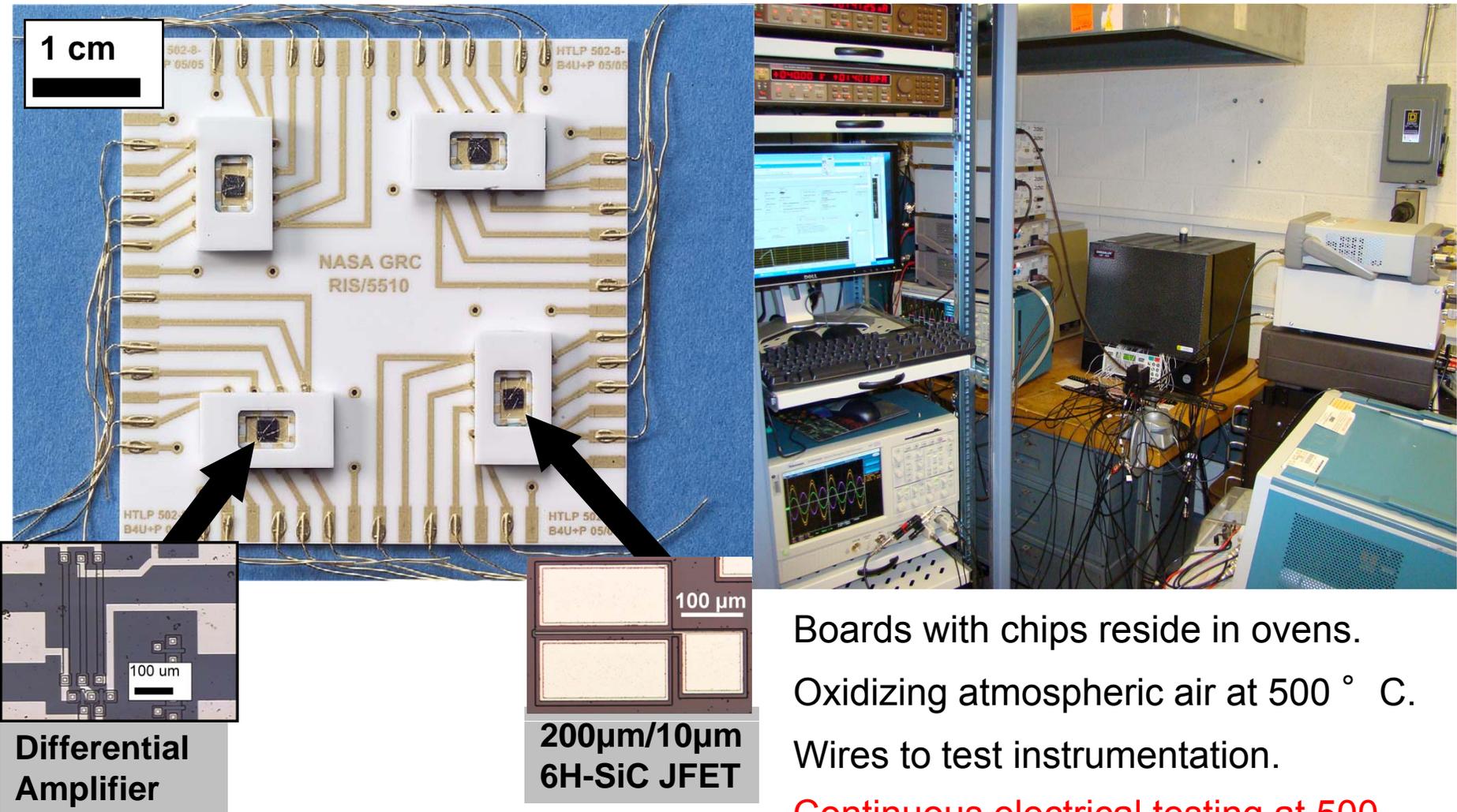
Packaged with bond wires





Packaged Devices and Test Setup

Parallel fabrication and testing of both single-transistors and IC's



Boards with chips reside in ovens.
Oxidizing atmospheric air at 500 ° C.
Wires to test instrumentation.

Continuous electrical testing at 500 ° C.



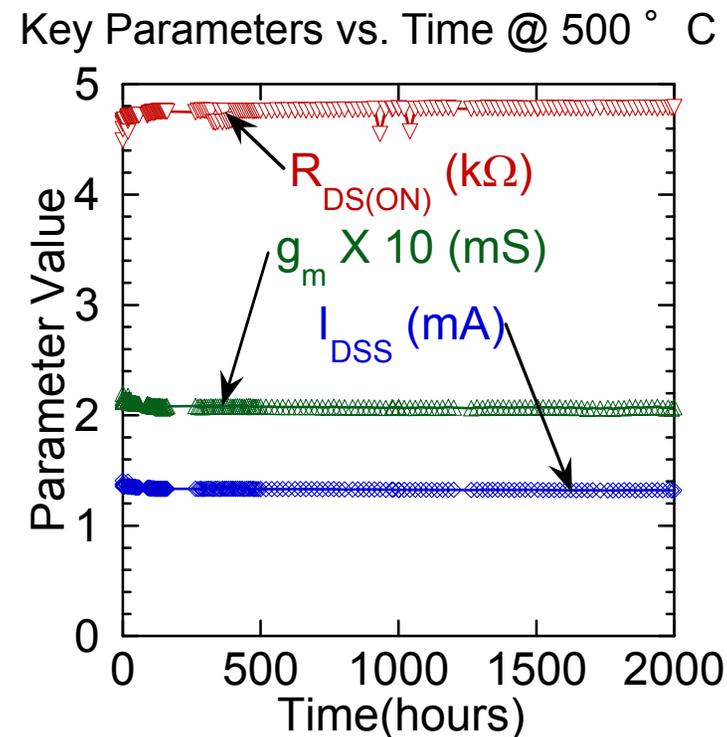
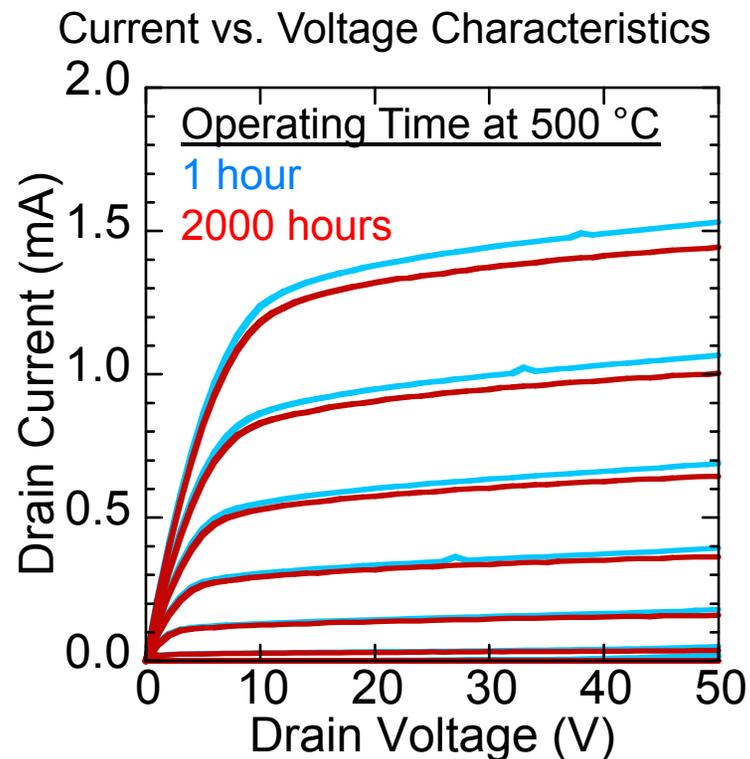
NASA Glenn SiC JFET : First Transistor to Surpass 2000 Hours of Stable Electrical Operation at 500 ° C

Current-voltage characteristics are very good and stable after 2000 hours.

- Enables realization of analog integrated circuits (amplifiers, oscillators).

Excellent turn-off characteristics, large ON to OFF current ratio (> 1000).

- Enables realization of digital logic circuits.



Less than 7% change occurs during 2000 hours at 500 ° C (most during 1st 100 hrs)
- 7% change is smaller than listed on most silicon transistor spec. sheets.



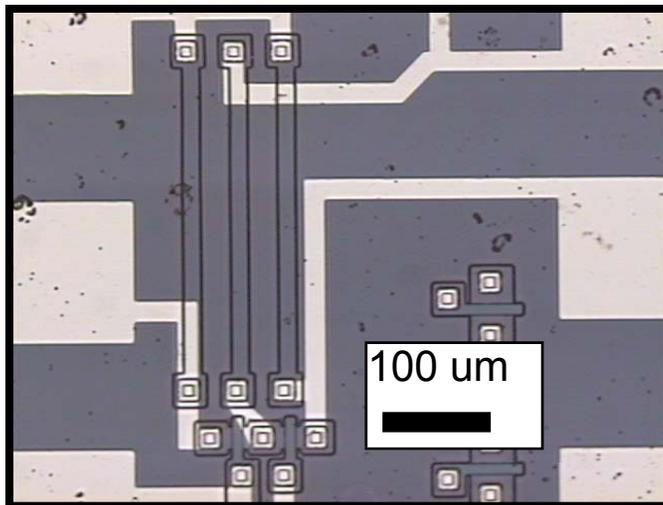
NASA Glenn Silicon Carbide Differential Amplifier

Tech Accomplishments
(IVHM v1.5 MS 1.3.5)

World's First Semiconductor IC to Surpass
2000 Hours of Electrical Operation at 500 ° C

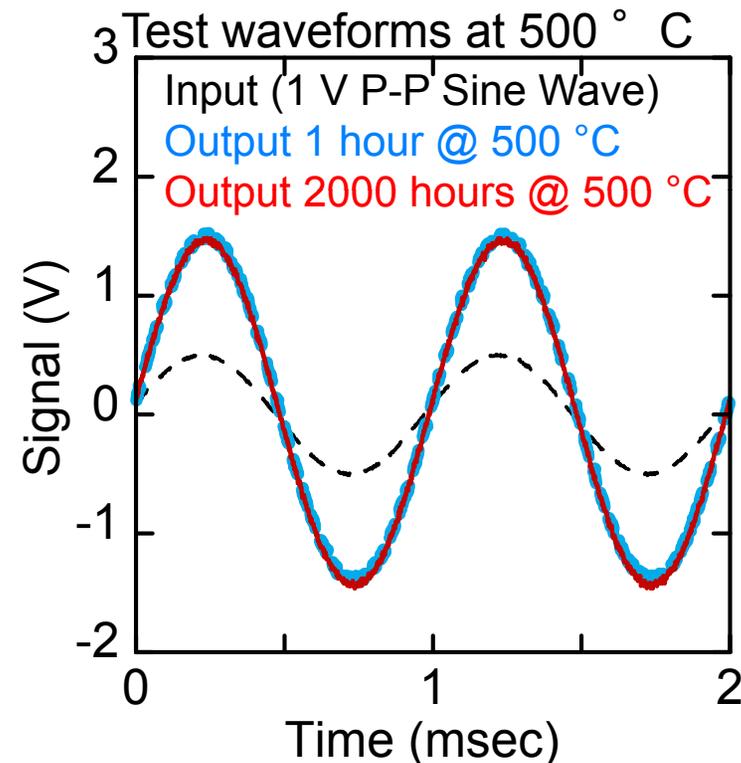
Demonstrates CRITICAL ability to interconnect transistors and other components (resistors) in a small area on a single SiC chip to form useful integrated circuits that are durable at 500 ° C.

Optical micrograph of demonstration amplifier circuit before packaging



2 transistors and 3 resistors
integrated into less than half a
square millimeter.

Single-metal level interconnect.



Less than 3% change in
operating characteristics during
2000 hours of 500 ° C operation.

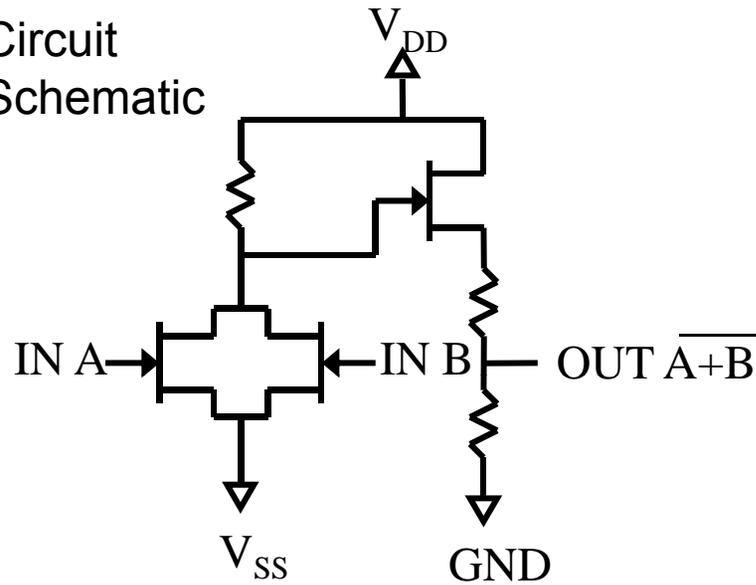


NASA Glenn SiC JFET NOR Gate IC

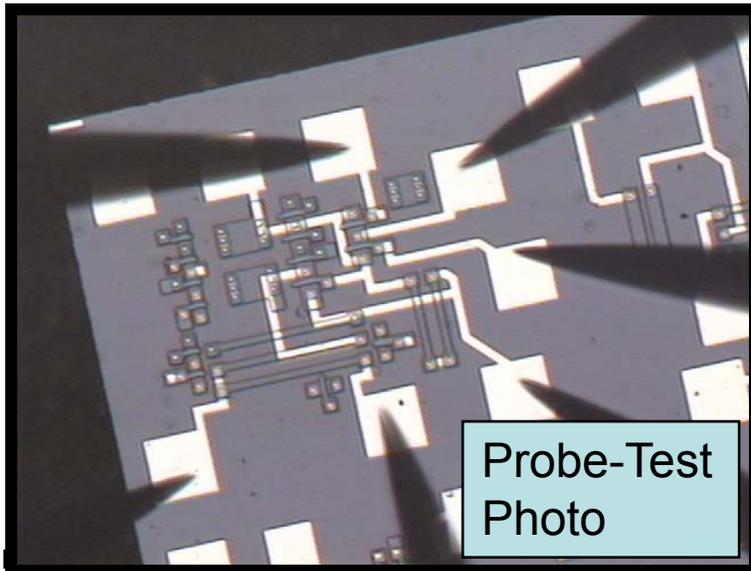
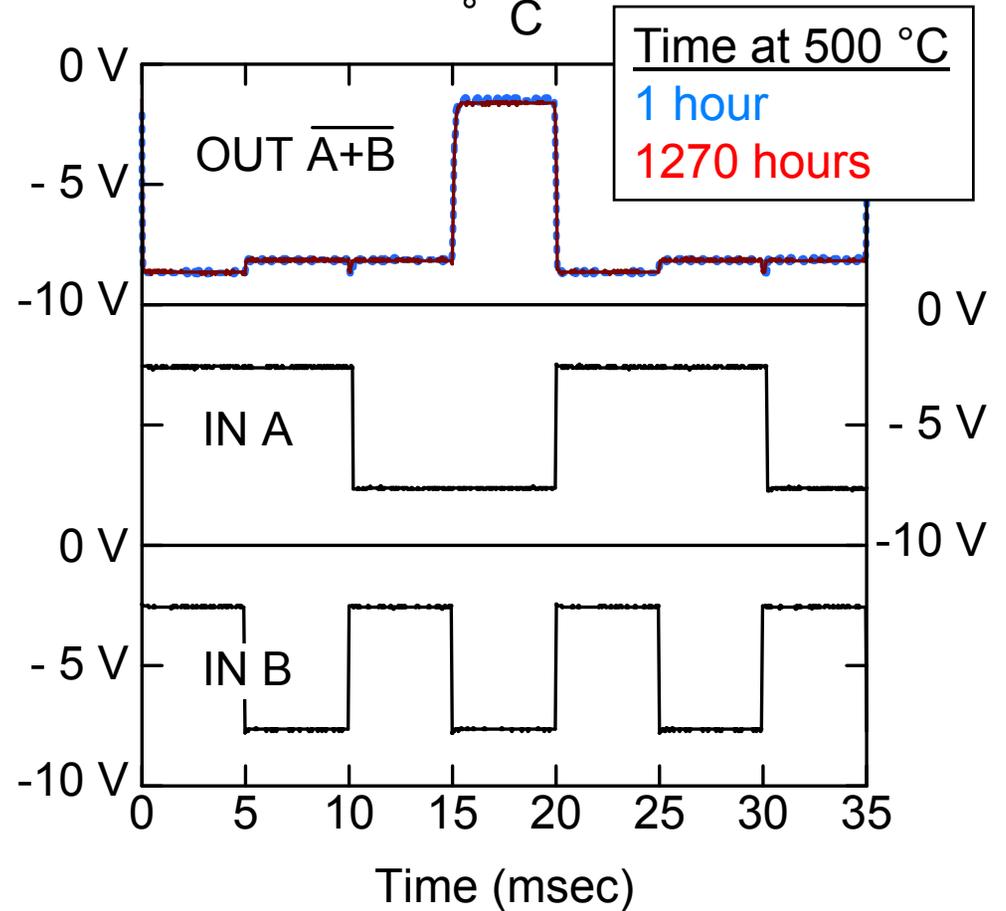
Tech Accomplishments
(IVHM v1.5 MS 1.3.5)

**World's First Semiconductor Digital IC to
Surpass 1000 hours of 500 ° C Operation**

Circuit
Schematic



Waveforms of **packaged**
NOR (= "Not OR") gate at 500
° C





Next Steps for SiC IC Development

1. Continue high temperature testing.
 - How long will the chips last at 500 ° C?
 - Analyze failure mechanisms (after circuits finally fail).
 - Revise process to further increase 500 ° C circuit durability.
 - Test more chips, test at 600 ° C (accelerated failure testing).
 - Test for thermal cycling, thermal shock, vibration, etc.
2. Improve metal interconnects from single-level to double-level process.
 - Enable much more complicated integrated circuitry.
3. Fabricate improved SiC transistors and prototype integrated circuits.
 - Higher frequency operation (shrink devices, antennas & passives).
 - Up-scaled levels of integration (100's to 1000's of transistors).
 - Complete 500 ° C wireless telemetry integrated circuits.
 - Engine ground test and flight demonstrations.
 - Demonstrate even higher temperature operation.
4. Transfer technology for further development and manufacturing.



Summary

**NASA has pioneered revolutionary durable 500 ° C integrated circuits.
New technology foundation -- new applications!**

**Durable high temperature IC's will enable important new
capability highly relevant to advancing IVHM.**

- Enabled by fundamental electronic materials research.
- **World record IC durability at 500 ° C (> 200-fold improvement).**
- Approach is inherently up-scalable to high circuit complexity while remaining physically small.

Further development should lead to beneficial technology insertion.

- IC's for engines (especially new wireless health monitoring).
- Technology transfer and commercialization.
- Additional applications (automotive, well-drilling, Venus).

Chips are still running well at 500 ° C.

- Amplifier chip went past 3000 hours on 10/31/07.